

REMARKS

Applicant amends claims 14 and 22 to correct minor informalities.
Accordingly, claims 12-24 remain pending in the application.

Reexamination and reconsideration are respectfully requested in view of the following Remarks.

35 U.S.C. § 103

The Office Action rejects claims 12, 13 and 18 under 35 U.S.C. § 103 over Ooishi U.S. Patent 5,835,436 (“Ooishi”) in view of Conley et al. U.S. Patent 6,426,893 (“Conley”); claims 14-16 and 19-24 over Ooishi in view of Conley and further in view of Hazen et al. U.S. Patent 6,088,264 (“Hazen”); and claim 17 under 35 U.S.C. § 103 over Ooishi in view of Conley and Hazen and further in view of Abedifard et al. U.S. Patent 6,665,221 (“Abedifard”).

Applicant respectfully traverses all of those rejections for at least the following reasons.

Claim 12

Among other things, the Flash memory of claim 12 includes a content addressable memory array coupled to receive a logical signal from an external device for comparison with defect addresses stored in the content addressable memory array; a memory array having word lines coupled to respective match lines of the content addressable memory array, wherein response to activation of one of the match lines, the memory array outputs a substitute address signal representing a substitute address stored in a row corresponding to the activated match line; and multiplexing circuitry connected to select between the logical address signal and the substitute address signal as a physical address signal, the multiplexing circuitry providing the physical address signal for selection of a memory cell being accessed

The Office Action fairly concedes that Conley does not disclose such features. However, the Office Actions states that Ooishi discloses such features and that “[i]t

would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate [such features from Ooishi] in Conley's Flash memory."

Applicant respectfully disagrees. Applicant respectfully submits that one skilled in the art would not have been motivated to make the proposed modification of Conley, as such a modification would have changed the principle of operation of Conley, and furthermore would not have been suggested because the redundancy block addressing means of Ooishi would have been generally unsuitable for a device such as that disclosed by Conley.

At the outset, M.P.E.P. § 2143.01 provides that:

"THE PROPOSED MODIFICATION CANNOT CHANGE THE PRINCIPLE OF OPERATION OF A REFERENCE. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)."

Here, the proposed modification of Conley to include the redundancy block addressing means of Ooishi would change the fundamental principle of operation of Conley and is therefore, improper. Conley's fundamental principle of operation is based upon the use of separate, designated, overhead (OH) blocks in each Unit which identify defective blocks and which directly specify the addresses of any replacement block (see, e.g., FIGs. 10 and 12; col. 2, lines 56-65; col. 13, line 61 – col. 14, line 11 ("*as part of the present invention, however, this type of information is stored in another block*"); col. 14, line 66 – col. 15, line 9; col. 15, lines 20-24; claims 1, 8, 20, 21, 22; the Title. Therefore, the proposed modification would change this fundamental principle of operation of Conley's invention.

Also, in any event, one of ordinary skill in the art would not have been motivated to modify Conley to include the redundancy block addressing means of Ooishi. Ooishi is directed to a DRAM device which has a very small number of very large “blocks” (e.g., 64 Mbit blocks) (see col. 61, line 57 – col. 62, line 3). In that case, the sizes of the memory required for the mapping memory and the address conversion unit are very small relative to the size of the memory device itself, resulting in negligible overhead. In contrast, Conley is directed to a FLASH memory device which has a very large number of very small blocks defined by the cells spanning a single erase line (e.g., 512 bytes per block). In that case, the sizes of the memories that would be required for the mapping memory and the address conversion unit would be larger relative to the memory device itself, resulting in a more substantial overhead.

For all of these reasons, Applicant therefore respectfully traverses the proposed combination of Conley with Ooishi as being improper and lacking any suggestion in the prior art.

Also among other things, the memory blocks of the device of claim 1 store parameters, code and data.

Applicant sees nothing in Conley disclosing that it is adapted to store any code in memory blocks. In that regard, Applicant respectfully notes that “Boot Info” is “system boot information” or “data” (e.g., physical address of reserved block 0), and not code as featured in claim 1 (see col. 16, lines 53-60; col. 17, lines 1-8).

Accordingly, for at least these reasons, Applicant respectfully submits that the device of claim 12 is patentable over the prior art.

Claim 13

Claim 13 depends from claim 12 and is deemed patentable over the prior art for at least the reasons set forth above with respect to claim 12.

Claims 14-16

Claims 14-16 depend from claim 12. Applicant respectfully submits that Hazen does not remedy the shortcomings of the prior art as explained above with

respect to claim 12. Accordingly, claims 14-16 are also deemed patentable over the prior art.

Claim 17

Claim 17 depends from claims 12, 14 and 16. Applicant respectfully submits that Abedifard does not remedy the shortcomings of the prior art as explained above with respect to claim 12. Accordingly, claim 17 is also deemed patentable over the prior art.

Claim 18

Among other things, the method of claim 18 includes storing defect addresses in a content addressable memory array in the Flash memory; storing substitute addresses in a memory array in the Flash memory; applying a first logical address from an external device to the content addressable memory array for a comparison operation; and outputting from the memory array a substitute address corresponding to a match line activated as a result of the comparison operation.

As explained above with respect to claim 1, Applicant respectfully submits that one skilled in the art would not have been motivated to make the proposed modification of Conley, as such a modification would have changed the fundamental principle of Conley's invention, and furthermore because the redundancy block addressing means of Ooishi would have been generally unsuitable for a device such as that disclosed by Conley. Accordingly, Applicant respectfully traverses the proposed combination of Conley with Ooishi.

Furthermore, Applicant respectfully submits that, contrary to the Office Action, Conley does not disclose storing parameters, code, and data in separate blocks of memory cells, wherein each of the blocks has a uniform size selected for parameter storage, as Applicant sees no suggestion in Conley of storing any code in any memory blocks.

Accordingly, for at least these reasons, Applicant respectfully submits that the method of claim 18 is patentable over the prior art.

Claims 19-24

Claims 19-24 depend from claim 18. Applicant respectfully submits that Hazen does not remedy the shortcomings of the prior art as explained above with respect to claim 18. Accordingly, claims 19-24 are deemed patentable over the prior art for at least the reasons set forth above with respect to claim 18, and for the following additional reasons.

Claims 19-21

Among other things, the methods of claims 19-21 all include applying a second logical address from the external device directly to a decoder in the Flash memory while applying the first logical address to the content addressable memory, wherein a combination of the first and second logical addresses identifies a memory cell.

Applicant respectfully submits that no such feature is disclosed or even remotely suggested in claim 13 of Ooishi, nor in any event does the Office Action even provide any proposed motivation to modify Conley (which only has two rows per block) to include such a feature. Therefore, Applicant respectfully traverses the proposed modification of Conley as lacking any suggestion in the prior art.

Accordingly, for at least these additional reasons, Applicant respectfully submits that claims 19-21 are patentable over the cited art.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 12-24, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283-0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No.

50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

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